

Abstract of the Disclosure

A semiconductor memory device includes a bitline equalizing voltage generator for using boost voltage. The semiconductor memory device includes a sense amplifier shared by a first memory block and a second memory block, bitline isolation circuits, bitline equalizing circuits, a bitline equalizing voltage circuit, and bitline equalizing signal generator. The bitline isolation selectively connects the first or second memory block with the sense amplifier in response to the first or second bitline isolation signals. The bitline equalizing circuits precharge the bitlines of the first and second memory blocks with bitline precharge voltage in response to the first and second bitline equalizing signals. The bitline equalizing voltage generator provides bitline equalizing voltage by reusing the boost voltage on the bitline isolation signal and thereby connects with bitline equalizing signal. Accordingly, since the voltage, which is discharging from the bitline isolation signal, is reused with the voltage to increase the bitline equalizing signal level, it is proper to use in the low power operation mode of the memory device. Likewise, during the low power operation, if external voltage comes to be low, the bitline equalizing signal rises as much as a certain level higher than the external voltage so that the bitlines can be precharged reliably.